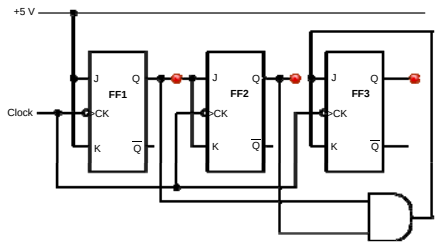
Synchronous Counters



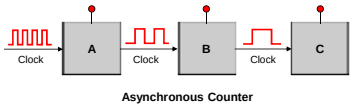
In this presentation you will:

- explore the operation of synchronous up and down counters
- discover the advantages and disadvantages of synchronous counters

Next >

Asynchronous and Synchronous Counters

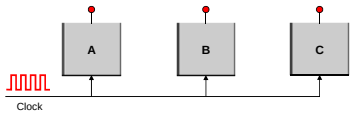
There are two main types of counter circuits, asynchronous and synchronous.



Asynchronous Counter

In an asynchronous counter, each stage is clocked by the previous stage.

In a synchronous counter, all stages are clocked at the same time.



Synchronous Counter

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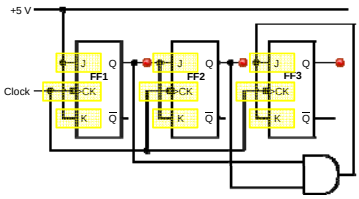
Synchronous Up Counter

This three-stage counter circuit uses J-K flip-flops.

Since all stages are clocked by the same external clock signal, this is a synchronous counter circuit.

Each J-K flip-flop will change state when a clock pulse occurs if its J and K inputs are both at logic 1.



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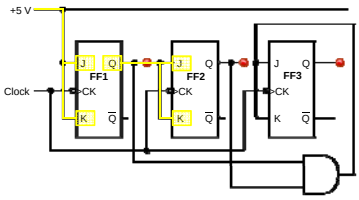
Synchronous Up Counter

The J and K inputs of FF1 are tied high, so FF1 will change state on every clock pulse.

The J and K inputs of FF2 are connected to the Q output of FF1, so FF2 will only change state when a clock pulse occurs if the output of FF1 is high.



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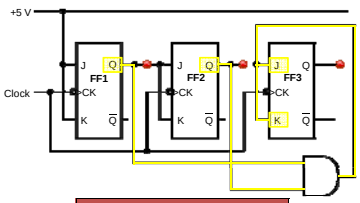
Synchronous Up Counter

The J and K inputs of FF3 are controlled by an AND gate whose inputs are the Q outputs of FF1 and FF2.

Therefore FF3 will only change state when a clock pulse occurs if the Q outputs of FF1 **and** FF2 are high.

The truth table shows the logic states of the Q outputs after each clock pulse.

The increasing binary code shows that this circuit is an up counter.



3-Stage Up Counter			
Clock Pulse	Logic State at Q		
	FF3	FF2	FF1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

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Question 1

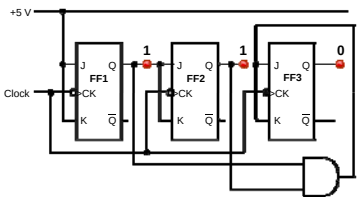
The Q outputs of this synchronous counter circuit are as shown. Which flip-flops will change state on the next clock pulse?

A) FF1 only

B) FF1 and FF2

C) FF1 and FF3

D) FF1, FF2 and FF3



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Question 1

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Which flip-flops will change state on the next clock pulse?

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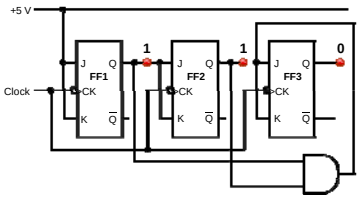

All three flip-flops change state because their J and K inputs are high when the clock pulse occurs.

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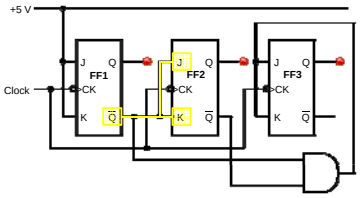
Synchronous Down Counter

The synchronous up counter circuit can be changed into a down counter by changing the input connections to FF2 and FF3.



The J and K inputs of FF2 are now connected to the $\overline{Q}$ output of FF1, so FF2 will only change state when a clock pulse occurs if the Q output of FF1 is low.

Next >

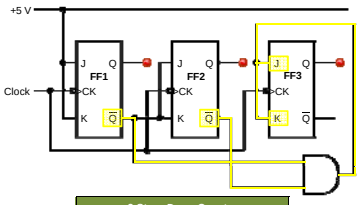
Synchronous Down Counter

The AND gate inputs are now connected to the $\overline{Q}$ outputs of FF1 and FF2.

Therefore FF3 will only change state when a clock pulse occurs if the Q outputs of FF1 and FF2 are both low.

Here is the new truth table for the counter.

The decreasing binary code confirms that this is a down counter.



3-Stage Down Counter			
Clock Pulse	Logic State at Q		
	FF3	FF2	FF1
0	0	0	0
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1

Next >

Question 2

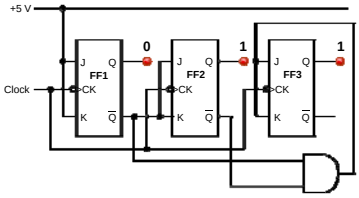
The Q outputs of this synchronous counter circuit are as shown.
Which flip-flops will change state on the next clock pulse?

A) FF1 only

B) FF1 and FF2

C) FF1 and FF3

D) FF2 and FF3



Next >

Question 2

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A) FF1 only

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C) FF1 and FF3

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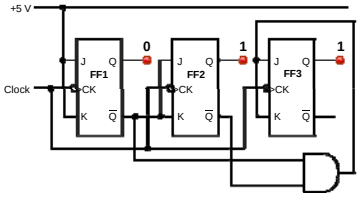

FF1 and FF2 change state because their J and K inputs are high when the clock pulse occurs. FF3 does not change state because its inputs are low.

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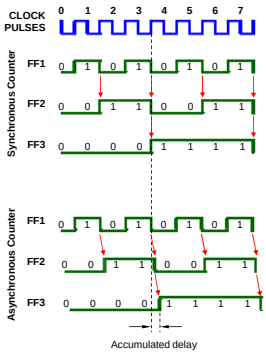
Advantages and Disadvantages of Synchronous Counters

Since all the stages of a synchronous counter are clocked at the same time, they do not suffer from the 'ripple effect' that occurs in asynchronous counters.

This makes them more suitable for applications where the timing of the counter circuit is critical.

The main disadvantage of synchronous counter circuits is that they are more complex than asynchronous counters.



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Question 3

Which of the following statements about synchronous counters is true?

A) They can only count down.

B) They use simpler circuits than asynchronous counters.

C) There is no 'ripple effect' between stages.

D) Each stage of the counter clocks the next.

Next >

Question 3

Which of the following statements about synchronous counters is true?

A) They can only count down.

B) They use simpler circuits than asynchronous counters.

 C) There is no 'ripple effect' between stages.

D) Each stage of the counter clocks the next.

Next >

Summary

In this presentation you have seen:

- how to construct synchronous up and down counters
- the advantages and disadvantages of synchronous counters

End